Amendments to the Claims:

Please cancel claim 2, amend claims 1, 3, 15 and 16, and add new claim 21 as shown in the following listing of claims. This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (currently amended) A driver circuit comprising:

an output transistor connected between a voltage terminal and an output node to produce an output signal on said output node, said output transistor including a control terminal;

a current source connected to said control terminal of said output transistor to provide a reference current~~, said current source being configured to generate said reference current proportional to a reference voltage and a reference frequency~~; ~~and~~

a memory operatively connected to said control terminal of said output transistor, said memory being configured to store a signal on said control terminal of said output transistor from a previous operating cycle in which said output transistor was activated; and

a feedback capacitor connected from said output node to said control terminal of said output transistor to control said output transistor as a function of a difference between current through said capacitor and said reference current.

2. (canceled).

3. (currently amended) The driver circuit of claim 1 [[2]] wherein said memory includes a memory capacitor and an amplifier, said amplifier being connected to said memory capacitor and said output transistor such that said amplifier is selectively configured in a voltage follower configuration to store said signal on said control terminal of said output transistor in said memory capacitor.

4. (original) The driver circuit of claim 3 further comprising a controlled switch located between said memory capacitor of said memory and said control terminal of said output transistor, said switch comprising a control input connected to said output node.

5. (canceled).

6. (previously presented) The driver circuit of claim 1 wherein said current source includes a frequency-to-current converter.

7. (original) The driver circuit of claim 1 further comprising a first switch located between said voltage terminal and said output transistor and a second switch located between said current source and said control terminal of said output transistor, said first and second switches being controlled by an input signal.

8. (original) The driver circuit of claim 1 further comprising:

a second output transistor connected between said output node and a second voltage terminal, said second output transistor including a control terminal;

a second current source connected to said control terminal of said second output transistor; and

a second feedback capacitor connected from said output node to said control terminal of said second output transistor.

9. (original) A driver circuit comprising:

an output transistor connected between a voltage terminal and an output node to produce an output signal on the output node, said output transistor including a control terminal;

a memory connected to said control terminal of said output transistor, said memory being configured to store a signal on said control terminal from a previous operating cycle in which said output transistor was activated;

a current source connected to said control terminal of said output transistor to provide a reference current; and

a feedback capacitor connected from said output node to said control terminal of said output transistor to control a rate of signal change on said output node.

10. (original) The driver circuit of claim 9 wherein said memory includes a memory capacitor and an amplifier, said amplifier being connected to said memory capacitor and said output transistor such that said amplifier is selectively configured in a voltage follower configuration to store said signal on said control terminal of said output transistor in said memory capacitor.

11. (original) The driver circuit of claim 10 further comprising a controlled switch located between said memory capacitor of said memory and said control terminal of said output transistor, said switch comprising a control input connected to said output node.

12. (original) The driver circuit of claim 9 wherein said current source is configured to generate said reference current proportional to a reference voltage and a reference frequency.

13. (original) The driver circuit of claim 12 wherein said current source includes a frequency-to-current converter.

14. (original) The driver circuit of claim 12 further comprising a first switch located between said voltage terminal and said output transistor and a second switch located between said current source and said control terminal of said output transistor, said first and second switches being controlled by an input signal.

15. (currently amended) The driver circuit of claim 9 further comprising:

a second output transistor connected between said output node and a second voltage terminal, said second output transistor including a control terminal;

a second memory connected to said control terminal of said second output transistor, said second memory being configured to store a signal on said control terminal of said second output transistor from a previous operating cycle when said second output transistor was activated;

a second current source connected to said control terminal of said second output transistor to provide a second reference current; and

a second feedback capacitor connected from said output node to said control terminal of said second output transistor to control a second rate of signal change on said output node.

16. (currently amended) A method for driving an electrical device, said method comprising:

receiving an input signal;

applying a stored signal to an output transistor in response to said input signal to produce an output signal on an output node connected to said output transistor; and

controlling said output signal on said output node using a difference between a reference current and current capacitively fed back from said output node.

17. (original) The method of claim 16 further comprising storing a control signal on said output transistor as said stored signal.

18. (original) The method of claim 16 wherein said controlling includes generating said reference current using a reference frequency and a reference voltage, and applying said reference current to a control terminal of said output transistor.

19. (previously presented) The method of claim 16 further comprising:

applying a second stored signal to a second output transistor in response to said input signal to change said output signal on said output node; and

controlling said output signal on said output node using a difference between a second reference current and a second current capacitively fed back from said output node to said second output transistor.

20. (original) The method of claim 19 further comprising alternately activating said output transistor and said second output transistor.

21. (new) The driver circuit of claim 1 wherein said current source is configured to generate said reference current proportional to a reference voltage and a reference frequency.